

Data Sheet August 1, 2008 FN4591.2

Radiation Hardened Quad Differential Line Driver

Intersil's Satellite Applications FlowTM (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil HS-26C31RH-T is a Quad Differential Line Driver designed for digital data transmission over balanced lines and meets the requirements of EIA Standard RS-422. Radiation Hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26C31RH-T accepts CMOS inputs and converts them to RS-422 compatible outputs. This circuit uses special outputs that enable the drivers to power-down without loading down the bus. Enable and disable pins allow several devices to be connected to the same data source and addressed independently.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the HS-1840ARH-T are contained in SMD 5962-96663. A "hot-link" is provided from our website for downloading.

www.intersil.com/military/

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.

http://rel.intersil.com/reports/search.php

Features

- QML Class T, Per MIL-PRF-38535
- Radiation Performance
 - Gamma Dose 1 x 10⁵ RAD(Si)
 - SEU and SEL Immune to 100MeV/mg/cm²
- EIA RS-422 Compatible Outputs (Except for IOS)
- · CMOS Compatible Inputs
- High Impedance Outputs when Disabled or Powered Down
- Low Power Dissipation 2.75mW Standby (Max)
- Single 5V Supply
- Low Output Impedance 10Ω or Less
- Full -55°C to +125°C Military Temperature Range

Applications

• Line Transmitter for MIL-STD-1553 Serial Data Bus

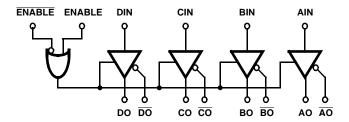
Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	PART MARKING #	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
5962R9666301TEC	HS1-26C31RH-T	Q 5962R96 66301TEC	-55 to +125	16 LD SBDIP	D16.3
HS1-26C31RH/PROTO	HS1-26C31RH/PROTO	HSI - 26C31RH/PROTO	-55 to +125	16 LD SBDIP	D16.3
5962R9666301TXC	HS9-26C31RH-T	Q 5962R96 63201TEC	-55 to +125	16 LD FLATPACK	K16.A
HS9-26C31RH/PROTO	HS9-26C31RH/PROTO	HS9 - 26C31RH/PROTO	-55 to +125	16 LD FLATPACK	K16.A

Pinouts

HS1-26C31RH-T HS9-26C31RH-T (16 LD SBDIP), CDIP-T16 (16 LD FLATPACK), CDFP4-F16 TOP VIEW TOP VIEW AIN 16 VDD AIN [16 □ VDD 15 DIN ΑО A0 🗖 2 15 DIN ĀŌ 14 DO 3 AO [14 J DO ENABLE 4 13 DO ENABLE [13 □ DO 12 ENABLE ВО 5 ENABLE 12 11 CO во во г 6 11 CO 10 CO 7 o co BIN [10 BIN 7 8 ☐ CIN GND [GND 8 9 CIN 9

Logic Diagram



TRUTH TABLE

DEVICE POWER ON/OFF	INPUTS			OUTPUT	
	ENABLE	ENABLE	IN	OUT	OUT
ON	0	1	Х	HI-Z	HI-Z
ON	1	Х	0	0	1
ON	Х	0	0	0	1
ON	1	Х	1	1	0
ON	Х	0	1	1	0
OFF (0V)	Х	Х	Х	HI-Z	HI-Z

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Die Characteristics

DIE DIMENSIONS:

 $2450\mu m \times 4950\mu m \times 533\mu m \pm 25.4\mu m$ (97 x 195 x 21mils $\pm 1mil$)

METALLIZATION:

M1: Mo/Tiw Thickness: 5800Å M2: Al/Si/Cu

Thickness: 10kÅ ±1kÅ

SUBSTRATE POTENTIAL:

Internally connected to $V_{\mbox{\scriptsize DD}}$. May be left floating.

BACKSIDE FINISH:

Silicon

PASSIVATION:

Type: SiO₂

Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm²

TRANSISTOR COUNT:

285

PROCESS:

Radiation Hardened CMOS, AVLSI

Metallization Mask Layout

HS-26C31RH

